Nanoscale Potential Measurements of Grain boundaries in Pentacene Thin Film Transistors and KPFM Image Reconstruction

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We present a comprehensive Kelvin probe force microscopy (KPFM) study of Pentacene thin film transistors with different film thicknesses in combination with current-voltage measurements and three dimensional electrostatics simulations. It is found that in Pentacene films thinner than approximately 30nm, holes are accumulated in the grain boundaries (resulting in upward band bending, see Figure 1 (b)) induced by negative trapped charge at the SiO_2-Pentacene interface. On the other hand, in films thicker than approximately 30 nm we observe hole depletion (downward band bending) mainly due to charge trapping in the grain boundaries. The results are discussed in view of their effect on Pentacene thin film transistors performance.

The last part of the talk will describe our progress in developing algorithms and methods to deconvolute KPFM measurements conducted at small tip-sample distances.

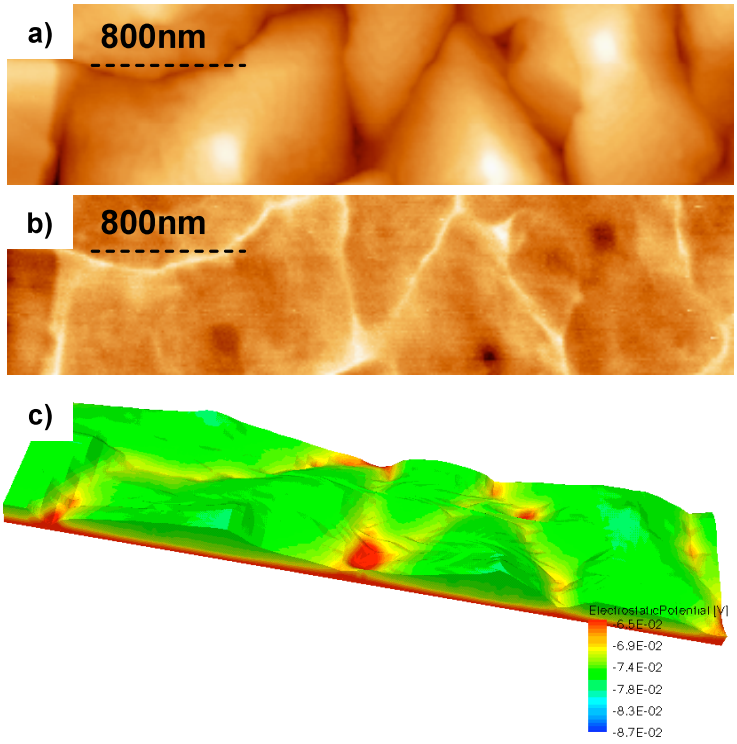

Figure 1: a) Topography b) measured CPD and c) calculated CPD in 3D of 30nm thick Pentacene film. The images were measured at V_g=0.

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